Research on Development of High Precision Frequency Stability Meter

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Abstract: With the application of high-precision frequency sources in industrial production, military and high-tech fields, it is particularly important to accurately measure the frequency stability of high-precision frequency sources. Therefore, it is of great significance to improve the accuracy of the frequency stability meter. The high-precision frequency stability meter described in this paper adopts the same accuracy frequency measurement method, which takes the output signal of the developed high-precision frequency source as its reference clock source, to ensure the high precision of the measurement system reference source. Compared with the frequency multiplication method widely used presently, this study simplifies the hardware circuit greatly and independently develops a comprehensive software system, which has a wide range of market value.

1. Introduction

From the perspective of the international development trend, the frequency stability standard has been raised very fast, of which index has been increased by an order of magnitude for almost 6 to 8 years [1]. With the improvement of the accuracy of these frequency sources, the accuracy of frequency stability measurement is getting higher and higher, and so far it has been reached 10^{-15} abroad [2]. However, the domestic study started relatively late (the study about quartz crystal oscillator started in the early 1960s), after that a series of high-precision frequency standard has been developed. With the improvement of the signal frequency standard, there has been corresponding progress made in the measurement of frequency stability [3]. The devices for the time-domain and frequency-domain stability comparison measurements are also increasing in number, of which accuracy are getting higher and higher. In particular, the extremely precise time is required in the fields of radar, navigation, missiles, space exploration and space flight, and the technology advancement in these fields cannot be separated from the development of high-precision and high-stability frequency sources. In recent years, the frequency stability index has been raised to or even higher [4].

All of our existing communications systems and equipment have a frequency source, reference frequency source or signal source, and their quality directly affects the reliability and non-stop communication system. Low frequency stability will lead directly to communications poor signal quality, or out-of-sync communication can result in inaccurate communication capabilities [5]. Therefore, frequency stability is one of the key technologies of many communication systems. As a measure of frequency stability, the measurement tool of the technology is very important with a wide range of market value of the technology. This paper comes from the atomic frequency standard high-precision frequency synthesis of the development project, and the main content of this paper is to design a high-precision frequency stability measurement system. The paper studies the definition and characterization of frequency stability and causes the instability of frequency. Based on the analysis of various frequency stability measurement techniques and frequency multiplier principle, the designed test circuit combined with single-chip technology is presented. In addition, the test system to achieve high precision is simple, which takes into account the operation and provides intuitive measurement results.

2. Systematic Technology

2.1 Structural Characteristics of Frequency Stability Measurement

As shown in Figure 1, this design uses self-developed high-precision frequency source as the input reference frequency standard, doubled to 100MHz by the high-precision frequency multiplier circuit, the buffer and the shaping circuit shaping into a standard square wave, the output as a FPGA DDS Module trigger clock, and then by the DDS output 10.000090MHz sinusoidal signal, and the measured clock output of the 10MHz sinusoidal signal sent to the mixer, and then filtered by a low-pass filter, buffer amplification and shaping to get a square wave signal of about 90Hz , By the FPGA and other precision frequency measurement module for frequency measurement. Measured after multiple sets of data were passed to stm32 microcontroller to calculate the frequency stability of the data obtained by the LCD screen.

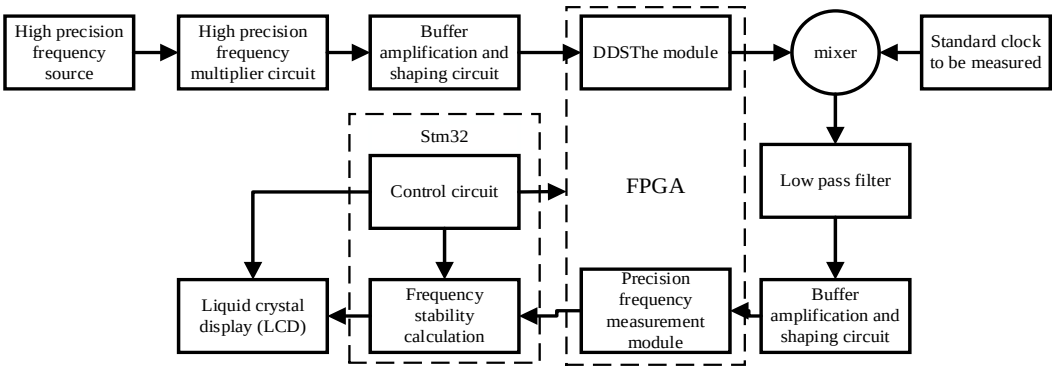

Fig.1 Structure of Frequency Stability Measurement

2.2 Multiplier Circuit Design

Frequency multiplier transistor selection. In the transistor selection, we must first consider the performance of the transistor must meet the frequency multiplier output frequency, output power and other indicators. The maximum operating frequency is generally guaranteed to be much larger than the frequency of the output signal of the frequency doubler. It can be seen from the manual, double gate field effect transistor 3SK223 typical amplifier circuit work in 470MHz, when the multiplier output is 100MHz, JT = 4.7J0, can well meet the design requirements. Compared with the bipolar transistor, the FET has the prominent advantages of high characteristic frequency, low noise, high input impedance, radiation resistance and high stability to environmental changes. Especially double-gate FET, the second gate has a good gain controllable characteristics, to further improve its frequency multiplier performance.

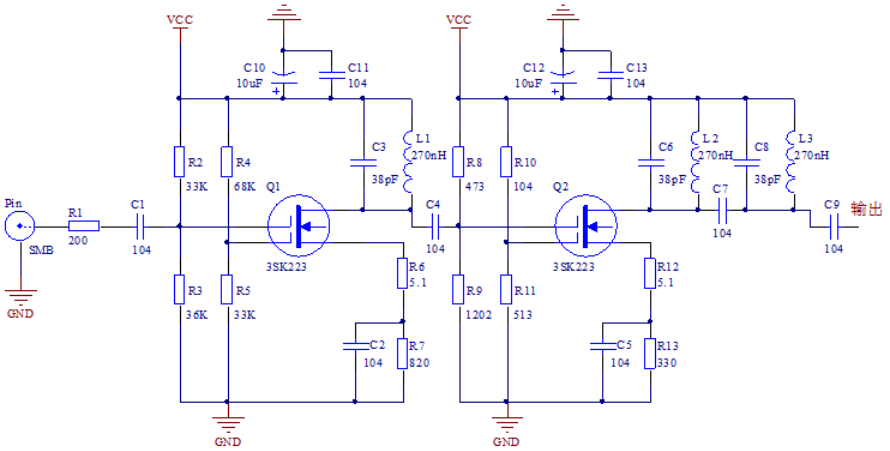

Fig.2 Multiplier Circuit Diagram

Resonance filter circuit design. For the frequency doubler to obtain higher efficiency and output power, in addition to the correct choice of bias and excitation strength, you must design good input and output matching, filtering network. One of the commonly used forms of matching networks is in the form of a parallel resonant circuit and the other is a matching network in the form of a filter. The second is mainly used for high-power, broadband, low-impedance output stage, or for varactor, step-tube multiplier input matching circuit. This section uses a parallel resonant circuit matching circuit. Through the parallel resonant circuit to obtain the frequency selection characteristics, through the transformer primary coil than the required impedance transformation relationship to meet the matching conditions.

Double frequency circuit overall design. The system needs 10 times the frequency of 10MHz signal. Taking into account the first harmonic there is a great difficulty, mainly harmonic amplitude is too small. Multi-level multiplication method to achieve multiple frequency function. The circuit diagram is presented as shown in Fig.2.

2.3 Mixing Circuit Design

The choice of mixer. The performance of the mixer determines the success of the mixer module design [6]. Taking into account the system requirements, need a small size, additional noise, with a certain bandwidth mixer. After comprehensive consideration, the choice is the TDK CB346M1A series mixer, with small size, good bandwidth characteristics, there is no induced noise, long life, low cost and so on.

Mixer output circuit selection. Taking into account the mixer output signal is relatively weak in the mixer output and then add an active frequency selective amplification to improve the output power of the signal and the final stage of the mixer circuit to increase the filter shaping the output of the mixer Weak sinusoidal signal into a square wave signal can be embedded TTL level recognition. Be prepared for post-processing.

2.4 Functional Unit of FPGA Design

Frequency stability measurement FPGA part is divided into five functional units, the software platform is Quartus II, the first to write each unit with Verilog language and generate a single cell Symbol (Symbol File), and then the top of the module file (Block Diagram File) Each Unit File (Symbol File) connected together, and finally by configuring pins and compilation, so as to complete the entire digital logic circuit design.

Equal precision frequency measurement unit. Equal precision frequency measurement unit is based on the principle of equal precision frequency measurement method [7], respectively, design preset gate counter, standard signal counter, signal counter to be measured. Preset gate counter to the external clock as the count clock, the maximum count value of 1000000. If the external clock frequency is 100MHz, the preset gate time is 10ms; if the external clock frequency is 10MHz, the preset gate time is 100ms; if the external clock frequency is 1MHz, the preset gate time is 1s; if the external clock frequency is 100KHz, the preset gate time of 10s; can achieve different time periods of frequency stability measurement. Standard signal counter is a standard 100MHz signal for the count clock, the maximum count of 232. The count starts when the actual gate is open, and stops when the actual gate ends.

Frequency Unit. Divider unit is based on the counter to achieve frequency function. The unit uses multiple decimal counter nesting, to achieve ten times the frequency, a hundred times the frequency, a thousand times the frequency, so as to get the same precision frequency measurement unit required a variety of external clock gate. The frequency division unit's reference clock is 100MHz, can be easily obtained by frequency division 10MHz, 1MHz, 100KHz.

RAM Storage Unit. Due to the use of gap alendron to replace the gapless Allan variance should be met:

$$\frac{T-\tau}{\tau}<1\% \tag{1}$$

(T-τ is the interval of twice sampling time, τ is the sampling time). In order to avoid the influence of real-time data transmission on the accuracy of the Allan variance, the system uses the data to be stored in RAM first. After a complete sample is completed Then with the microcontroller for data transmission. RAM memory cells are generated directly from the Mega Wizard Plug-In Manager tool in the Quartus II software. Since 101 sets of data are sampled, the address width is selected by 7 bits; the data width is selected by 32 bits, which can be matched well with the 32-bit frequency data output by the equal precision frequency measurement unit. The RAM write clock is controlled by the actual gate signal of equal precision frequency measurement module, and the read clock is controlled by the singlechip

2.5 SPI Communication Unit

As the system between the FPGA and the microcontroller are 32-bit data transmission, although the parallel port transmission speed, but taking into account the limited FPGA and microcontroller I / O resources, so the use of serial communication protocol. SPI is a high-speed, full-duplex serial communication, including master / slave mode. The four signal lines are: Serial Data Input (MISO, Master Input, Slave Output), Serial Data Output (MOSI, Master Output, Slave Input), Shift Clock (SCK), Active Low Slave Enable Signal (CS).

Figure 3 shows the FPGA functional unit overall wiring diagram. 100MHz standard clock is the driving clock of each functional unit. Under the control of the singlechip, the gate clock selection unit sends out the desired gate clock frequency, the equal precision frequency measurement unit completes 101 times of sampling, and stores the data in the RAM. After the sampling is finished. The microcontroller sends the read clock to the RAM storage unit, drives the RAM storage unit to transmit data to the SPI communication unit, and communicates with the SPI communication unit to obtain the data to complete the calculation and display.

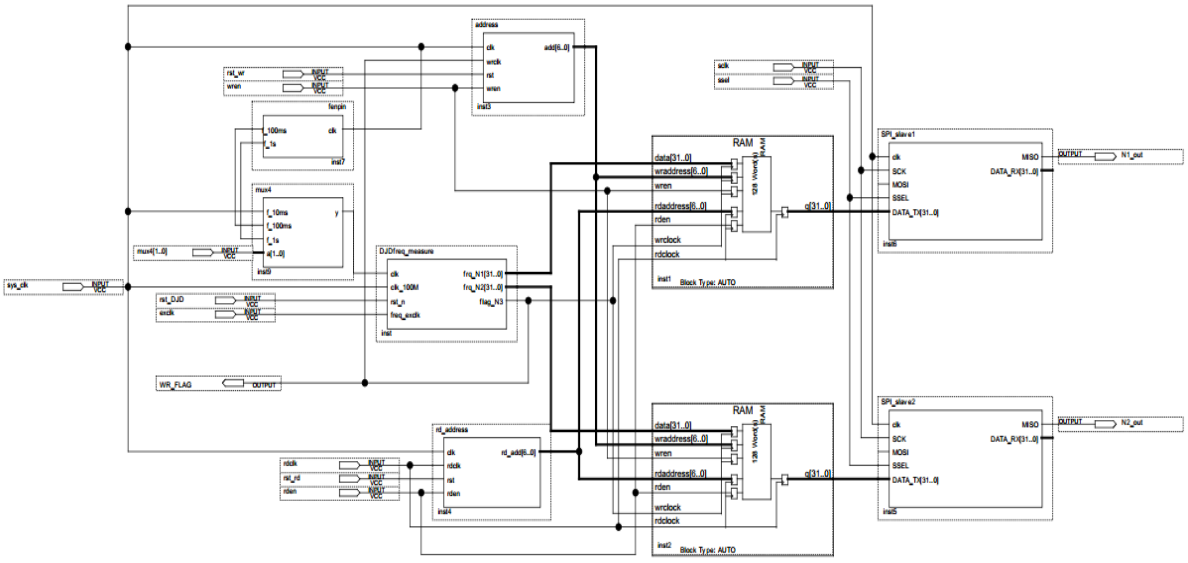

Fig.3 FPGA Functional Unit Overall Wiring Diagram

2.6 Single Chip Microcomputer Software Design

The stm32 microcontroller is considered as the control center in the system, and the main driver FPGA functional units, data transmission, data computing, liquid crystal display and other functions. Figure 4 is presented for the microcontroller software design flow chart.

First of all, initialize the configuration of each functional unit and I / O port, reset the write address, allow to write RAM, reset and other precision frequency measurement unit, and then start sampling. First to enable equal precision frequency measurement unit to monitor the actual gate is open, if the open, the sampling starts, and then monitor the actual gate is closed, if closed, the sampling is completed, then the FPGA internal data has been stored in RAM, the final reset precision measurement Frequency unit, ready for the next sample.

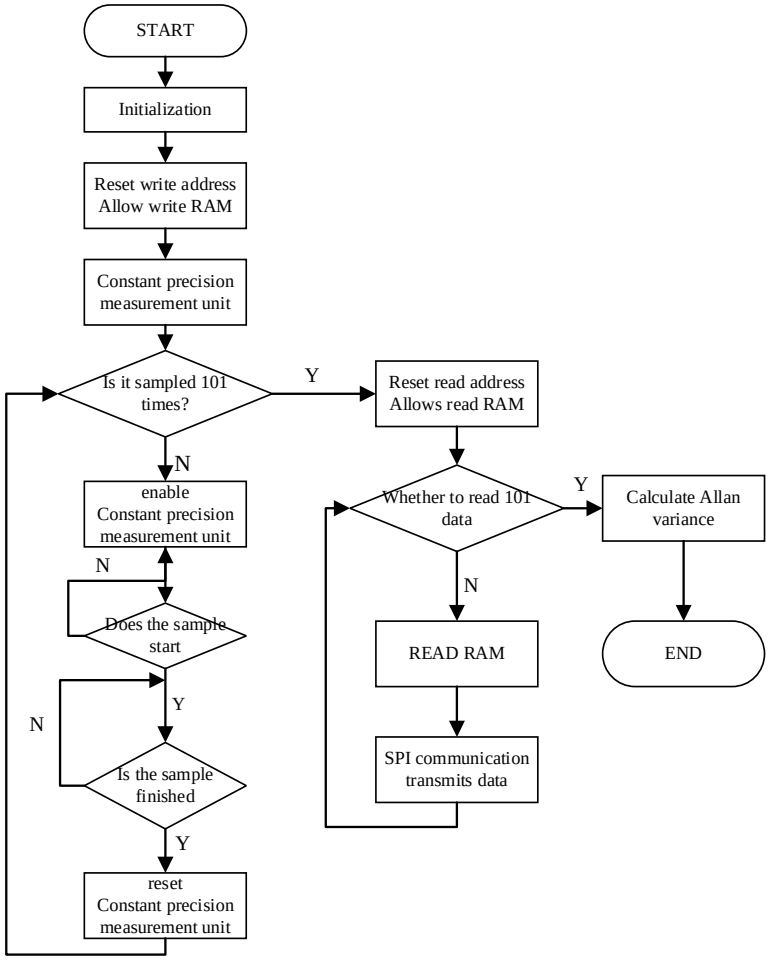

Fig.4 SCM software design flow chart

When the sample 101 times, the end of the sample. Reset read address, allowing read RAM, MCU control RAM memory cells and SPI communication unit for 101 times data transmission, and then carry out Allen calculation of variance, liquid crystal display. Figure 5 is the Allen variance calculation flow chart.

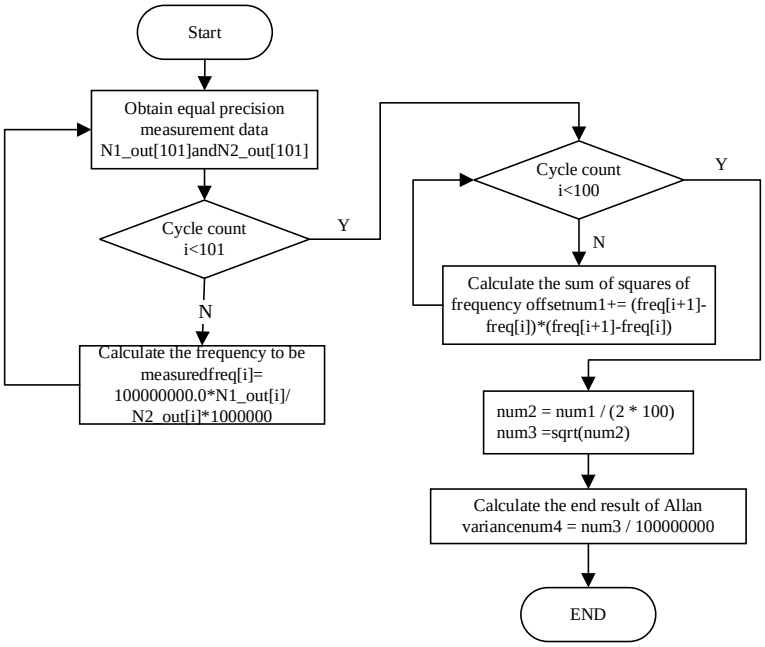

Fig.5 Allen variance calculation flow chart

3. System test results

Frequency stability measurement system performance parameters: During the system test, the signal under test is a high-precision temperature-compensated crystal oscillator. The measured results of the system are shown in Table 1. The data shows that the short-term frequency stability can reach 10^{-10}, reaching the basic specifications.

Tab.1 Measured Results of the System

Sampling Time / Test Order	10ms	100ms	1s	10s
1	1.1E-8	5.4E-9	9.3E-10	2.5E-10
2	1.3E-8	7.6E-9	8.0E-10	2.2E-10
3	9.8E-9	7.9E-9	9.0E-10	2.1E-10
4	9.9E-9	8.8E-9	8.5E-10	2.3E-10
5	1.0E-8	8.0E-9	8.4E-10	2.0E-10
6	9.5E-9	7.5E-9	8.6E-10	2.8E-10
7	9.7E-9	8.5E-9	8.2E-10	2.4E-10
8	1.1E-8	7.9E-9	8.7E-10	2.9E-10
9	1.5E-8	9.4E-9	8.9E-10	1.9E-10
10	9.9E-9	7.2E-9	8.9E-10	2.9E-10

4. Conclusion

This paper describes a system designed to measure frequency stability based on the frequency-difference multiplication method. The hardware circuit passed various tests and basically met the design requirements. At the same time, through the software part of the program can be very convenient to measure the design of long-term frequency stability measurement and measurement of short-term frequency stability of the program. The system will have a very high market value, which can be widely used to measure long-term frequency stability and short-term frequency stability of various signal sources, frequency synthesizer, crystal oscillator, atomic frequency standard. The paper introduces the hardware design method of each module in detail, and gives the schematic of circuit design. In double frequency module design, double tuned and double tuned are better than single tuned combo. Double-gate field effect transistor 3SK223 is selected at the same time, so the double frequency circuit has high stability, high input impedance, low noise, low noise Radiation ability and other prominent advantages. Mixing circuit using a diode stack CB346 and AD AD835 AD chip company, the chip into the high impedance, high output current, low noise, easy to design. Mixing, filtering amplification shaping, control of the display of each hardware module design process has taken corresponding measures to ensure that the system to meet the design requirement

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